University of Tabriz - Iran

(a paper describing)

CMOS-based carbon nanotube pass-transistor logic integrated circuits

by : Hamed Fooladvand / Supervised by : Dr. Abbasian

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Authors :

Li Ding[1,*], Zhiyong Zhang[1,*], Shibo Liang[1], Tian Pei[1], Sheng Wang[1], Yan Li[2], Weiwei Zhou[3], Jie Liu[3] & Lian-Mao Peng[1]

[1] Key Laboratory for the Physics and Chemistry of Nanodevices, and Department of Electronics, Peking University, Beijing, China.

[2] Key Laboratory for the Physics and Chemistry of Nanodevices, and College of Chemistry and Molecular Engineering, Peking University, Beijing, China.

[3] Department of Chemistry, Duke University, Durham, North Carolina, USA.

CONTENTS

INTRODUCTION

- Field-effect transistors based on carbon nanotubes have been shown to be faster and less energy consuming than their silicon counterparts. However, ensuring these advantages are maintained for integrated circuits is a challenge.

- Here we demonstrate that a significant reduction in the use of field-effect transistors can be achieved by constructing carbon nanotube-based integrated circuits based on a pass-transistor logic configuration, rather than a CMOS configuration.

INTRODUCTION

- Logic gates are constructed on individual carbon nanotubes via a doping-free approach and with a single power supply at voltages as low as 0.4 V.

- The pass-transistor logic configuration provides a significant simplification of the carbon nanotube-based circuit design, a higher potential circuit speed and a significant reduction in power consumption.

- In particular, a full adder, which requires a total of 28 field-effect transistors to construct in the usual CMOS circuit, uses only three pairs of n- and p-field-effect transistors in the pass-transistor logic configuration.

INTRODUCTION

An ideal design configuration for CNT-based ICs should fulfill the following two requirements:

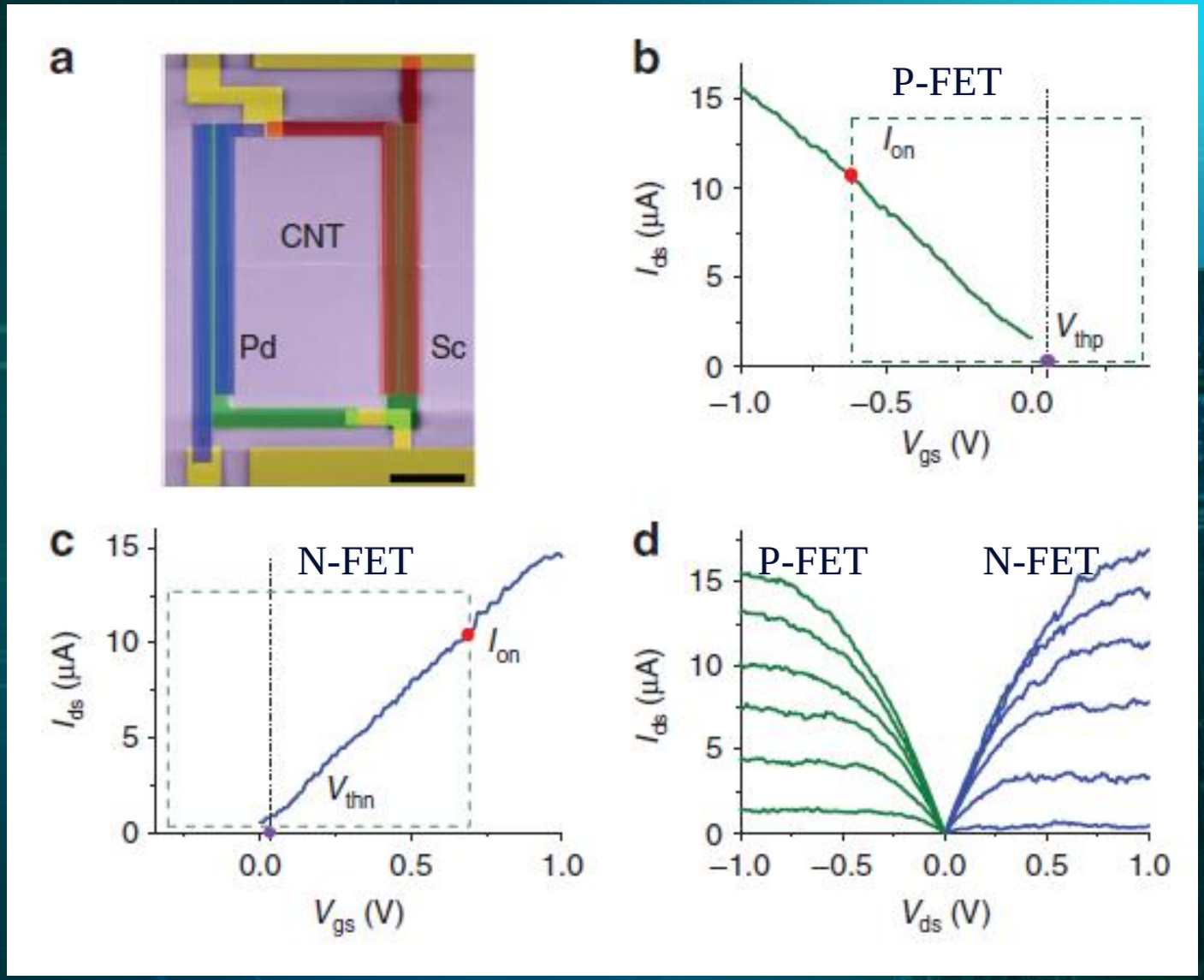
1. The first requirement is that circuit blocks designed with such a circuit configuration must possess sufficient signal gain and driving ability to guarantee signal fidelity and propagation in the circuit.

2. The second requirement is that the design configuration should take the full advantage of the superb properties of CNT-FETs and use as few transistors as possible while operating at higher speed and/or with lower power dissipation than conventional CMOS configurations.

Article Glance

- In this article, we focus on exploring a suitable circuit design configuration for CNT-based ICs, and constructing basic gates and more complex circuits for an ALU(Arithmetic & Logic Unit).
- At the physical level, high-performance CNT-based FETs are fabricated via a doping-free approach.
- At the architectural level, CNT-based ICs are designed following the configuration of a pass-transistor logic (PTL), which significantly reduces the number of transistors required.
- However, conventional Si-based PTL circuits encountered two major drawbacks; namely, threshold voltage drop and loss of gain, which have so far prevented PTL circuits from being widely used in ICs.
- Here we show that both drawbacks can be eliminated in CNT-based PTL circuits via threshold voltage engineering and combining PTL circuits with CMOS inverters.
- Basic logic gates such as OR and AND, as well as the more complex full adder, multiplexer (MUX) and demultiplexer (DEMUX) circuits are successfully fabricated on individual CNTs for the first time.

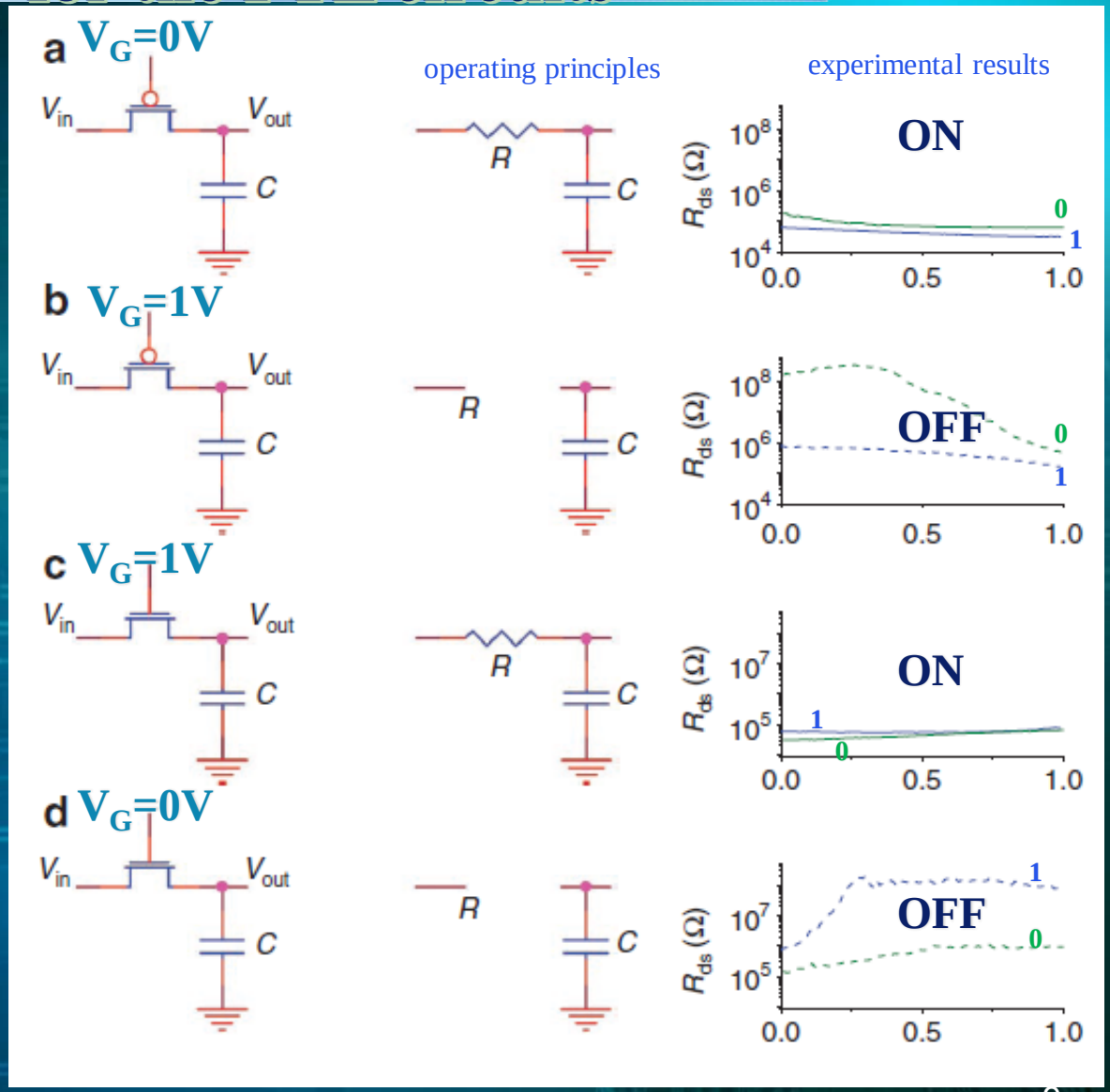
Device fabrication and characterisation



operating principles and experimental results for the PTL circuits

PTL

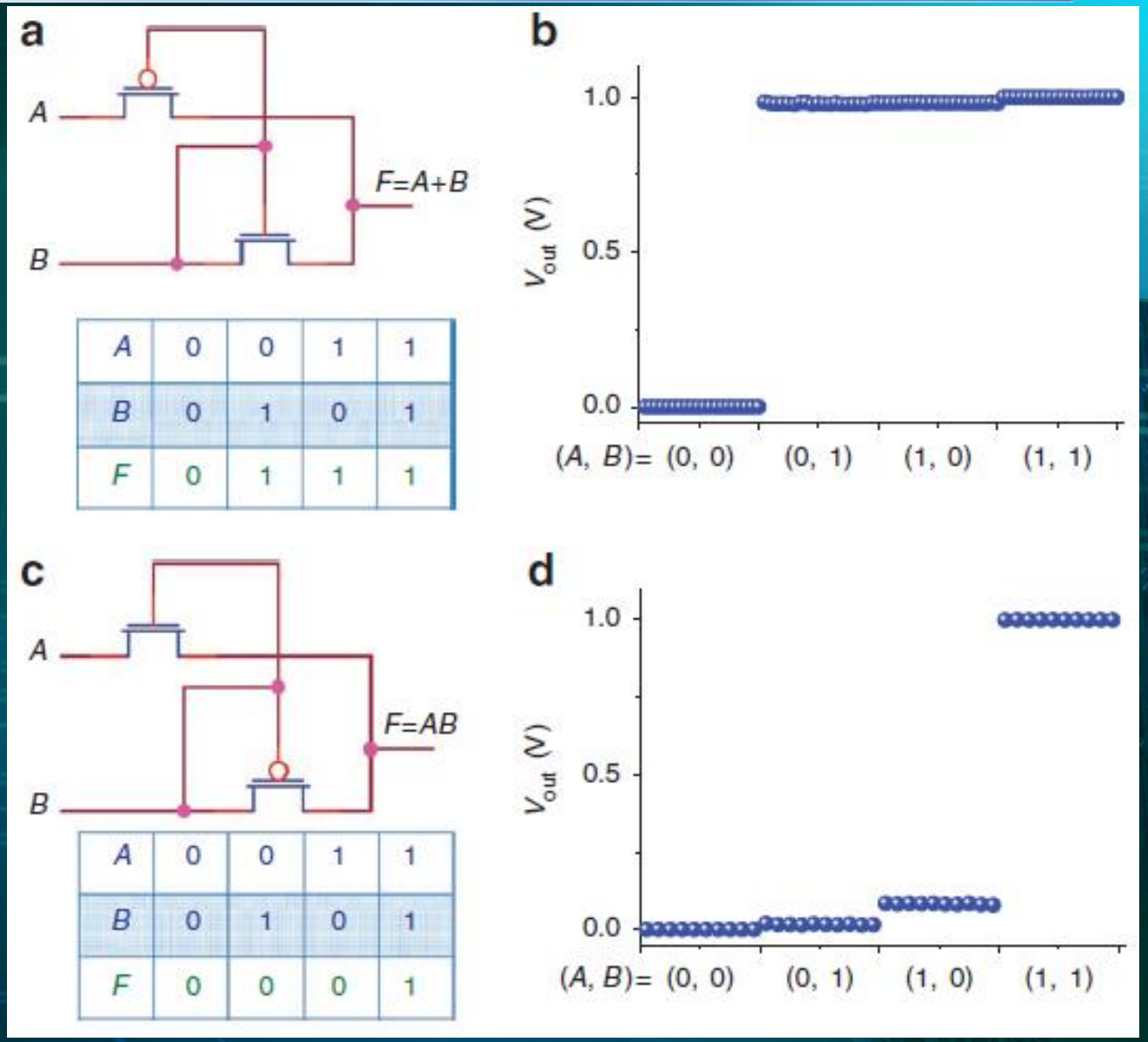
- **P-FET**
- **N-FET**



CMOS-based pass-transistor OR and AND gates

OR

AND

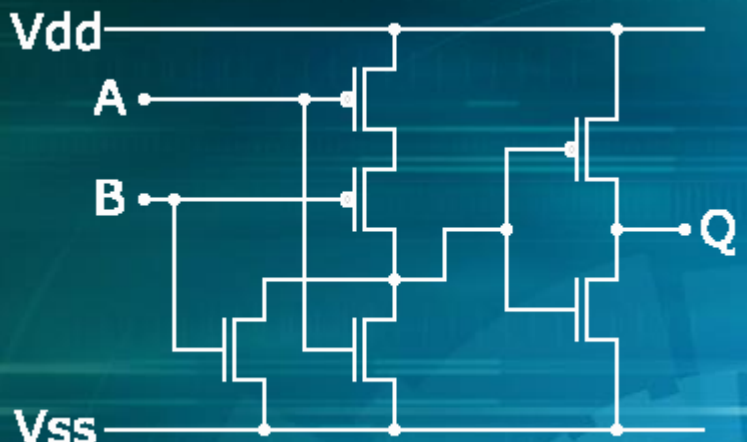


A	0	0	1	1
B	0	1	0	1
F	0	1	1	1

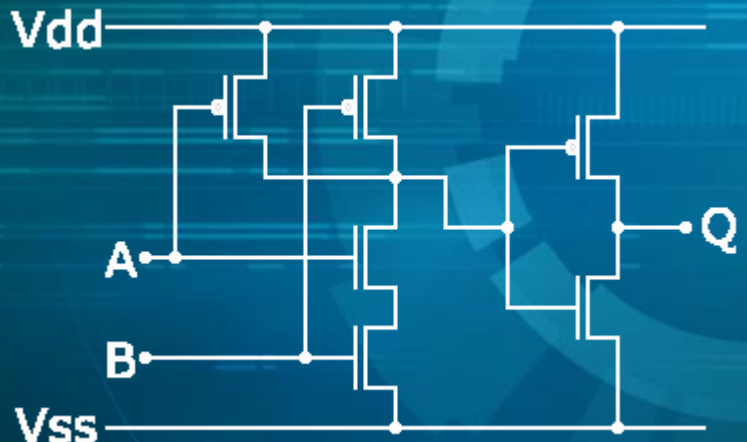
A	0	0	1	1
B	0	1	0	1
F	0	0	0	1

Conventional CMOS OR and AND gates

OR



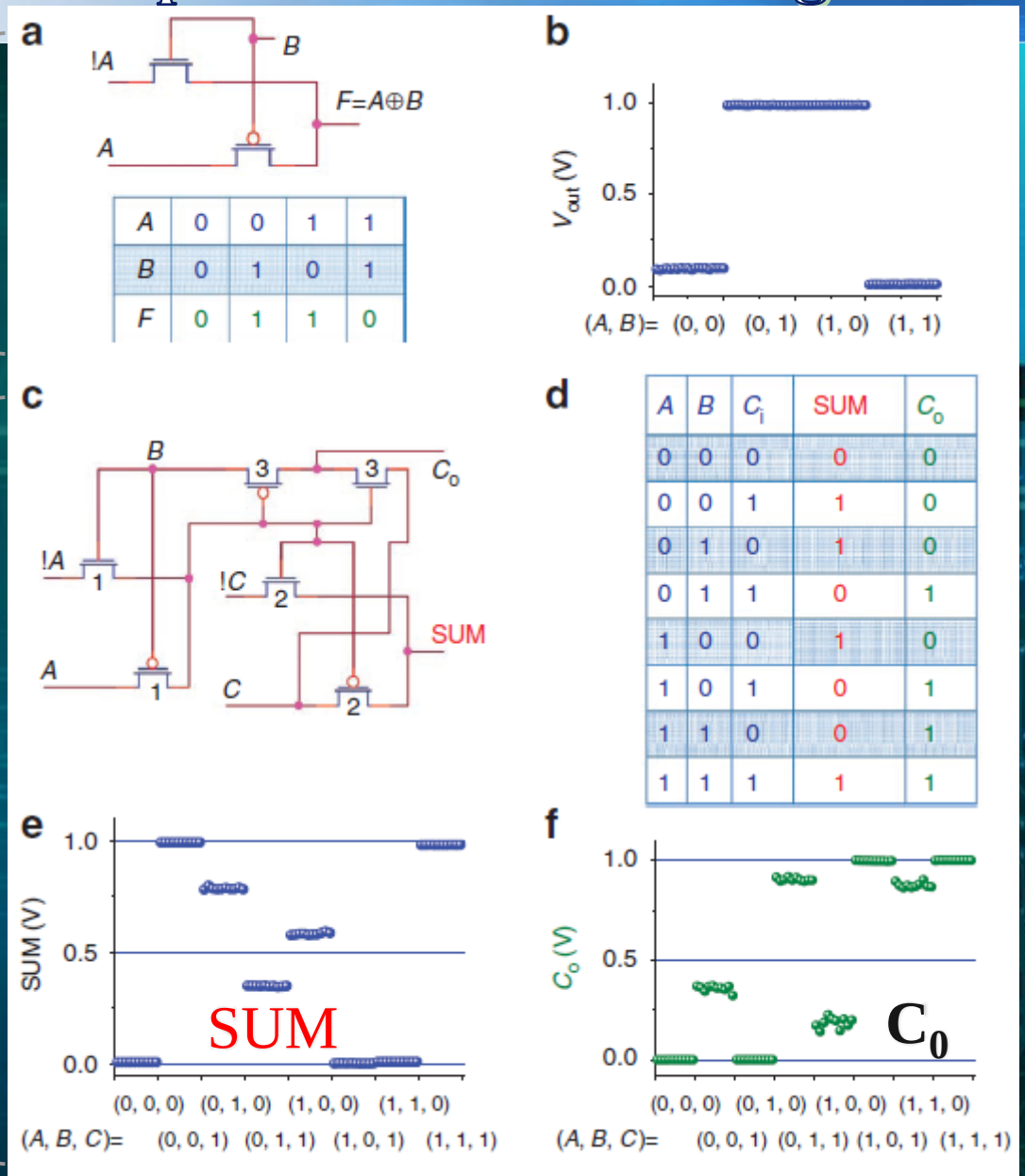
AND



CMOS-based pass-transistor XOR gate and a full adder

XOR

Full Adder

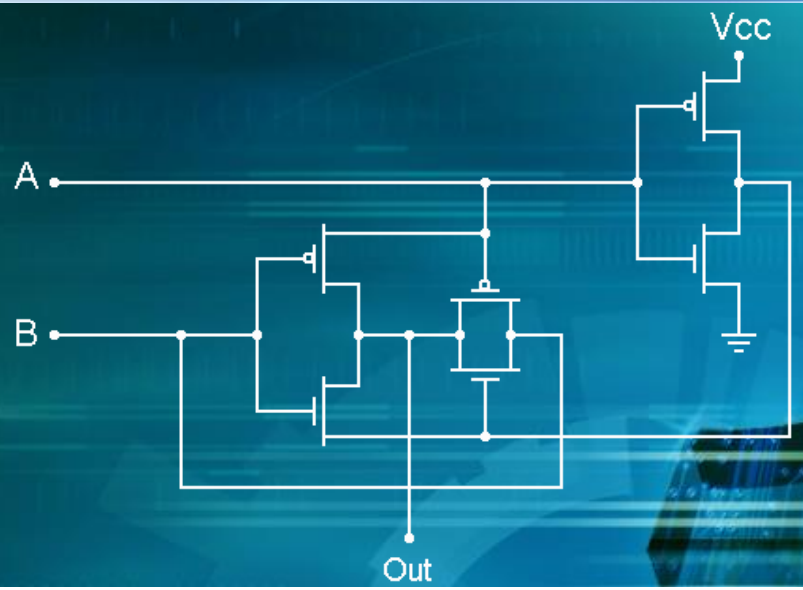


A	0	0	1	1
B	0	1	0	1
F	0	1	1	0

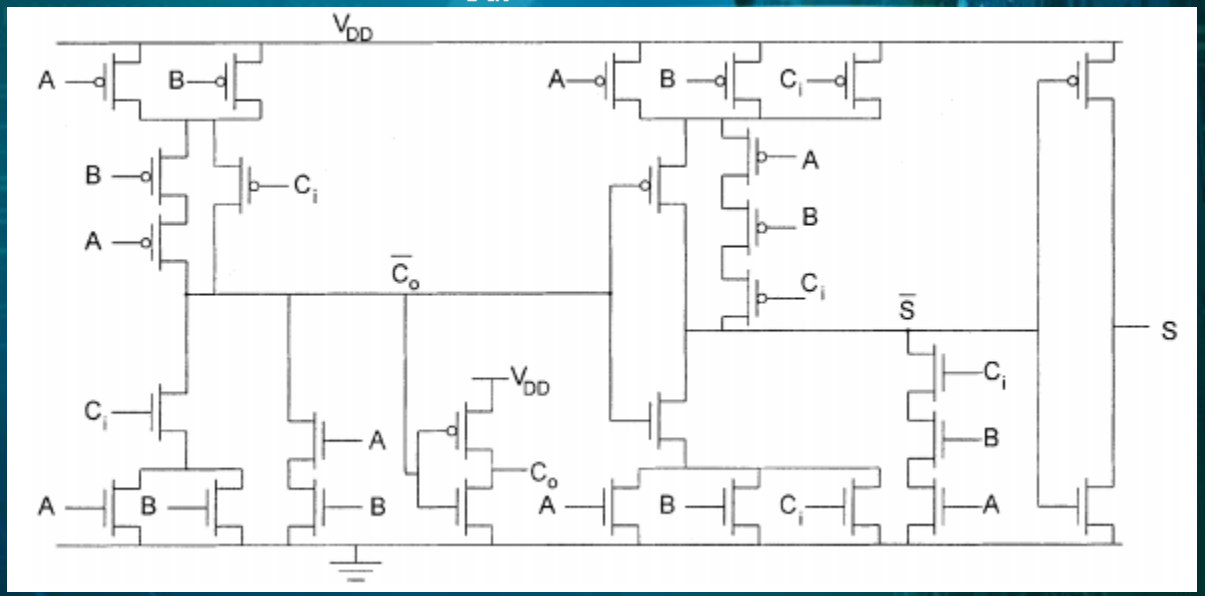
A	B	C_i	SUM	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Conventional CMOS XOR gate and a full adder

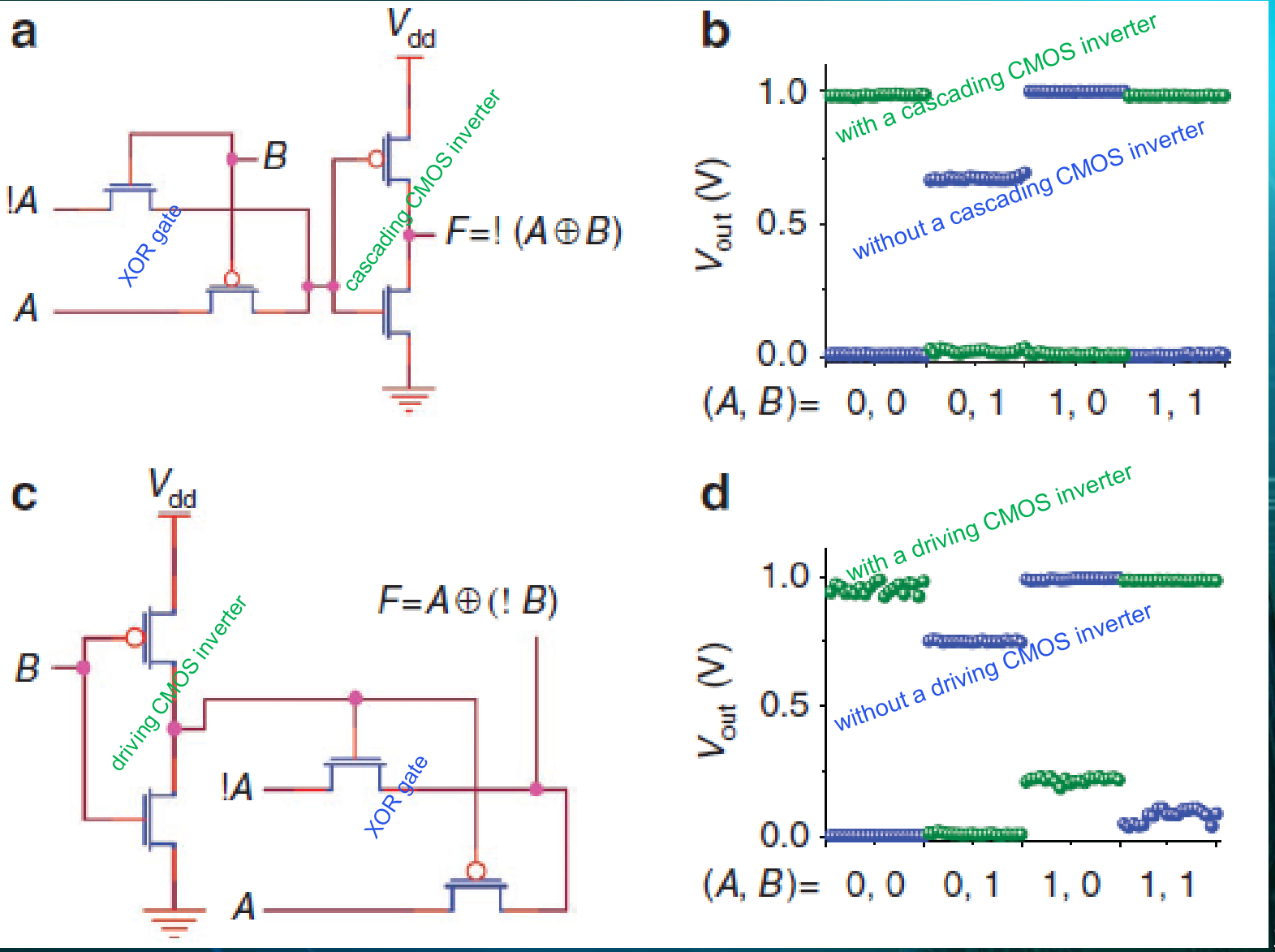
XOR



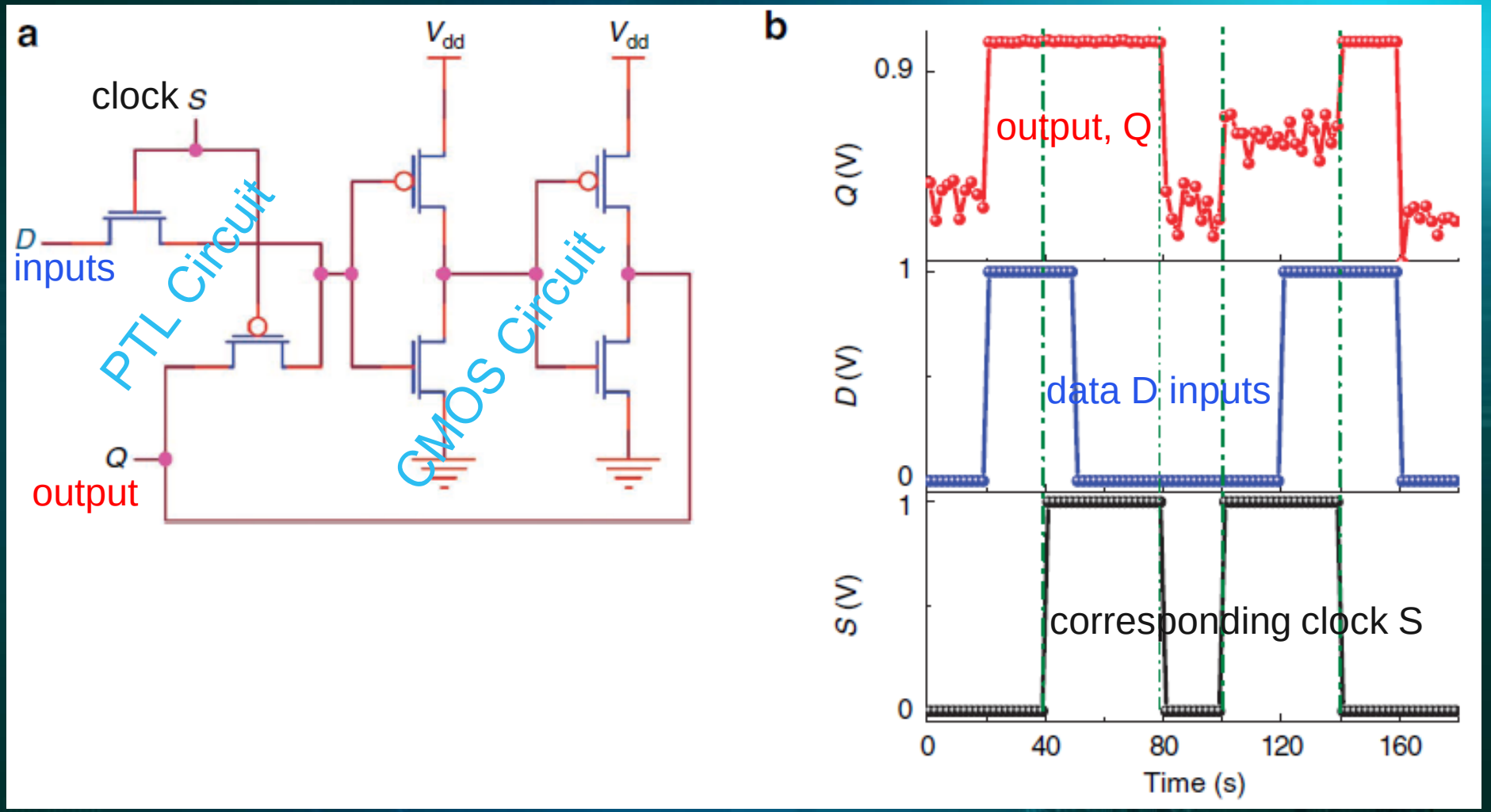
Full Adder



CMOS and PTL hybrid circuits



Design and characteristics of a CNT-based D-latch circuit



Conclusions

- The realisation of these circuits is sufficient for the construction of a **nano-ALU**.

- The realisation of these circuits is sufficient for construction of ICs with **faster** and **less energy consuming** in nano scale.

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Thanks a lot

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